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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/615,070 | 07/12/2000 | Hiroshi Makino | 49657-744 | 3244 |

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| EXAMINER |
|---|
| MYERS, PAUL R |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2189 | 8 |

DATE MAILED: 09/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/615,070 | MAKINO, HIROSHI | |
| | Examiner | Art Unit | |
| | Paul R. Myers | 2189 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *7/30/03* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 7/30/03 have been fully considered but they are not persuasive.

In regards to applicants argument that AAPA does not teach potential level of said bus node corresponding to the potential fixing circuit is transmitted to said data bus entirely: This is incorrect AAPA teaches that Japanese Patent Laying-Open NO. 63-85852 proposes a solution to the noise of the unfixed potential level problem of allowing the fixing of bus potentials when the bus is not used.

In regards to applicants argument that AAPA does not teach fixing the bus level when the data bus is not used: AAPA teaches the solution when the bus is not used.

In regards to applicants argument that figure 9 does not teach any bi-directional bus circuitry with a potential fixing circuit for setting the potential level of various bus nodes to a prescribed potential when data is not input to or output from any of a plurality of circuit blocks: The examiner agrees AAPA figure 9 teaches the multiple bus nodes while figure 10 teaches the potential fixing circuit.

In regards to applicants argument that AAPA figure 9 teaches the bus is in a floating state: The examiner agrees. However the AAPA also teaches this is a problem and teaches the use of a bus potential fixing circuit to alleviate this problem.

In regards to applicants argument that Figure 10 teaches a mono-directional bus: This is correct: However figure 9 teaches a bi-directional bus.

In regards to applicants argument that AAPA teaches away from combining the teachings of figure 9 with the teachings of figure 10 due to inherent difficulties. AAPA teaches the floating potential is a problem and the fixed potential of figure 10 is a solution thus it expressly teaches the motivation to combine the teachings of figure 9 with the teachings of figure 10.

2. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

The examiner notes the pervious examiners use of 35 USC 102 is appropriate in that all the claimed features are taught in a single reference. However since the AAPA teaches two different systems it would have been more appropriate to apply a single reference 35 USC 103 to combine the two systems in the single reference. Thus the rejection will be changed to a 103 rejection.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA).

5. As per claims 1 and 10, AAPA discloses a bi-directional bus circuitry (Fig. 9, 500; Specification page 1, lines 25-32) shared among a plurality of circuit blocks (Fig. 9, 10-a-d; Specification page 1, line 27 thru page 2, lines 3) comprising:

A data bus divided into (J+1) bus nodes (Fig. 9, Nb1, Nb2; Specification page 1, lines 27-29);

- each of said plurality of circuit blocks being connected to any one of (J+1) bus nodes (Fig. 9; Specification page 1, line 27 thru page 2, line 3);

- a potential fixing circuit provided corresponding to one of said (J+1) bus nodes, for setting a potential level of corresponding said bus node to a prescribed potential when data is input to/output from none of said plurality of circuit blocks (Fig. 10, 600; Specification page 3, line 30 thru page 4, line 17);

- J repeater circuits provided between adjacent said bus nodes respectively (Fig. 9, 50; Specification page 2, lines 4-11);

- each repeater circuit having

- a first signal transmitting circuit transmitting data from one to the other of said adjacent bus nodes (Fig. 9, 51; Specification page 2, lines 4-11), and

- a second signal transmitting circuit transmitting data from said the other to said one of said adjacent bus nodes (Fig. 9, 52; Specification page 2, lines 4-11); and

- an arbiter circuit receiving circuit block information for specifying a circuit block which is an object of data output, and controlling activation of said first and second signal transmitting circuits (Fig. 9, 520, 25; Specification pages 1, line 25 thru page 2, line 33),

AAPA Figure 9 does not teach said arbiter circuit activating, when said data is input to/output from none of said plurality of circuit blocks, either one of said first and second signal transmitting circuits in each repeater circuit, so that potential level of said bus node corresponding to said potential fixing circuit is transmitted to said data bus entirely. AAPA Figure 10 and page 3 lines 15-33 teaches activating, when said data is input to/output from none of said plurality of circuit blocks, a signal transmitting circuit, so that potential level of said bus node corresponding to said potential fixing circuit is transmitted to said data bus entirely. It would have been obvious to a person of ordinary skill in the art to apply AAPA figure 10 potential fixing circuit to all nodes of the repeater because this would have fixed the problem identified by AAPA figure 10 in the system of figure 9.

6. As per claims 2 and 11, AAPA discloses the claimed invention and furthermore teaches said first signal transmitting circuit includes a first tristate buffer controlled by the arbiter circuit and said second signal transmitting circuit includes a second tristate buffer controlled by the arbiter circuit (Fig. 9, 51, 52; Specification page 2, lines 4-33).

7. As per claims 3 and 12, AAPA discloses the claimed invention and furthermore teaches J is 1, with two bus nodes (Fig. 9, Nb1, Nb2); a first circuit block group connected to one node (10-a, 10-b); a second circuit block group connected to the other node (10-c, 10-d); the potential fixing circuit is corresponding to either one of bus nodes (Fig. 10; Specification, page 3, line 30 thru page 4, line 17); first signal transmitting circuit transmitting data from one of the nodes (Specification page 2, lines 4-33); second signal transmitting circuit transmitting data from the other of the nodes (Specification page 2, lines 4-33); and an arbiter circuit activates the first or

second signal transmitting circuit when data is output from none of the respective circuit blocks (Specification page 2, line 4 thru page 4, line 17).

8. As per claim 4, AAPA discloses the claimed invention and furthermore teaches data transmitted over the data bus has two states of high level and low level (Specification page 1, lines 29-32); the potential fixing circuit includes a switch circuit (Fig. 10, QTN) and an arbiter turns on the switch circuit when data bus is not used (Fig. 9, 520, 25, LG50, LG52).

9. As per claim 5, AAPA discloses the claimed invention and furthermore teaches a low level and an N-type transistor for switching(Fig. 10, QTN; Specification, page 1, lines 29-32, page 4, lines 1-17).

10. As per claim 6, AAPA discloses the claimed invention and furthermore teaches a high level (Specification page 1, lines 29-32). However, AAPA does not explicitly teach a P-type transistor for switching. Official notice is taken in that both the concepts and advantages of using P-type transistors for switching are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a P-type transistor for switching to match the system designer's requirements to connect the appropriate signal when the transistor is turned on or off.

11. As per claims 7-9 and 13, AAPA discloses the claimed invention and furthermore teaches the bi-directional bus circuitry for the case when J is 1. However, AAPA does not expand to the case when J is more than 1. Official notice is taken that both the concepts and advantages of duplicating the bi-directional circuitry for more bus nodes and bus repeater circuits are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at

the time of the invention to expand the system to handle any number of bus nodes and repeaters match the system designer's requirements and to provide an efficient system.

***Conclusion***

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305 3900.

Paul R. Myers

PRM
September 25, 2003

PAUL R. MYERS
PRIMARY EXAMINER